Arcadi Product Brief APB177

Ashling's ARC-core Emulators: Target Debug Connector Recommendations

Contents

1 Introduction

This document describes how to physically connect ARC-core target systems to Ashling Microsystems' emulation and debugging systems. Pin connection schemes are described for the ARC on-chip JTAG silicon module that provides the debug interface for ARC-core applications, for a user's ARC-core prototype implementation in a custom FPGA and for connection to ARC's ARCangel prototyping system.

In cooperation with ARC International, Ashling Microsystems supplies JTAG Emulators that operate with ARC's "SeeCode" Source Debugger, ARC-core customer boards and ARC's ARCangel prototyping system to provide a full debugging platform for ARC core applications.

Ashling's **Opella-ARC JTAG Emulator**, supplied and supported by Arcadi Systems, is used for debugging ARC cores or an ARCangel system with the ARC JTAG debug module; it includes a USB link to the host PC.

2 Choosing the right connection to your Target ARC application

Designers and system-integrators for ARC-core applications can use a variety of platforms for hardware and software debugging, system integration, and Verification and Validation:

1. SoC designs can be implemented by the designer in the form of an FPGA;
2. Initial prototyping of an ARC-core ASIC can also be carried out on ARC's ARCangel development platform (see section 7);
3. Debugging, integration and final Verification and Validation can be carried-out on the final custom silicon SoC.

The hardware interfaces for debugging each platform type are essentially the same; in all cases, the target must include the ARC-core JTAG debug IP module. However, there's one important difference: the hardware connection to ARCangel must allow programming (blasting) of configuration files to the FPGA.

For the hardware connection to your ARC target, Ashling offers a choice of Probe Cables:

1. **TPA-ARC-JTAG-20** 20-pin .1" JTAG probe cable, for connection to a 20-pin JTAG pin-strip on your custom target board; this cable can be used for debugging an ARC core in a custom FPGA or in final silicon. When used with Opella, this cable automatically adapts to target logic levels in the range 1.8V to 3.3V.

2. **TPA-ARC-JTAG-15** D15 JTAG probe cable, for connection to the D15 JTAG socket on the ARCangel prototyping unit: This cable must be used for debugging and FPGA blasting on ARCangel; it can also be used if you have included a D15 JTAG socket on your custom target board. This cable provides 3.3V logic levels, corresponding to the ARCangel's 3.3V interface logic levels.

3 ARC core Debug Connections

ARC cores (and the ARCangel prototyping system) implement a debug module that uses the JTAG serial interface.

3.1 Direct JTAG debug connection to ARC target systems

For use on an SoC design that has been implemented as a self-contained FPGA, *or* for debugging on a "real" ARC-core silicon SoC, you can use *either* the D15 JTAG Probe connections in section 3.2, *or* you can use the simpler 20-pin .1" connection arrangement in this section. Note that this 20-pin connector does not support FPGA blasting. When used with Opella this 20-pin probe automatically adapts to logic levels on the target debug interface in the range 1.8V to 3.3V.

Ashling's **TPA-ARC-JTAG-20** Target Probe Assembly contains a 20-pin double-row .1" female free socket that can connect to a male 20-pin JTAG pin-strip on your custom target board. Pin connections for this connector are shown in tabular form in Table 1.

Pins 4, 6, 8, 10, 12 and 14 on the Debug-probe are held at logic-low by the Opella-ARC JTAG Emulator; these pins should be connected to Ground on the target ARC system's JTAG debug-connector. (Earlier descriptions of this 20-pin ARC JTAG interface suggested that these pins be left open-circuited on the target debug connector. No adverse effects will occur if pins 4, 6, 8, 10, 12 and 14 pins are not connected; however, for future target-board design it's better to connect these pins to Ground on the target debug connector, as Table 1 recommends).

Pin	*Signal*	*Function*	*Direction*
1	Vtref	Target reference voltage; used by the Emulator to sense target voltage and adjust probe voltages accordingly (Note 1)	Output (from Target to Emulator)
2	(not used)	**(not used; do not connect to this pin)**	
3	TRESET*	Connect to Test Port Reset input (TRESET*) on ARC core, if available (active-low to reset the test port); **otherwise, do not connect to this pin** (Note 2)	Input (to Target from Emulator)
4	Logic-ground	Connect to Ground on Target (Note 3)	
5	TDI	JTAG Test Data In (Note 4)	Input (to Target from Emulator)
6	Logic-ground	Connect to Ground on Target (Note 3)	
7	TMS	JTAG Test Mode Select in (Note 4)	Input (to Target from Emulator)
8	Logic-ground	Connect to Ground on Target (Note 3)	
9	TCK	JTAG clock (Note 4)	Input (to Target from Emulator)
10	Logic-ground	Connect to Ground on Target (Note 3)	
11	RTCK	Connect to Returned JTAG Clock output (RTCK) on ARC target core, if available; otherwise, this pin can be connected to Ground on the target	Output (from Target to Emulator)
12	Logic-ground	Connect to Ground on Target (Note 3)	
13	TDO	JTAG Test Data Out	Output (from Target to Emulator)
14	Logic-ground	Connect to Ground on Target (Note 3)	
15	SRESET*	Target System Reset (Note 5) Connect to System Reset (SRESET*) on ARC target core system, if available (active-low to reset the target system); otherwise, do not connect to this pin	Bi-directional (Emulator Probe applies open-drain pull-down)
16	Reserved	Do not connect to this pin (+3.3V from Opella)	
17	Reserved	Do not connect to this pin	
18	GND	Connect to Ground on Target	
19	Reserved	Do not connect to this pin	
20	GND	Connect to Ground on Target	

Note 1: The Emulator applies a load of 200KΩ or greater (25μA or less) to Pin 1. This line should be connected to Vcc on the target board (a buffer resistor of not more than 100Ω can be used in series, but is not essential).

Note 2: Connect this pin to the Target's debug Test Port Reset line (active-low), if available. The Emulator drives TRESET* low to reset the Test Access Port. The Target may provide a pull-up to Vcc or a pull-down to ground on this pin (minimum 4.7KΩ, maximum 1mA) to provide a defined state when the Emulator isn't connected. If a Test Port Reset line is not available, do not connect to this pin.

Note 3: The Opella Emulator holds these pins at logic-low potential. Connect these pins to Ground on the target board.

Note 4: To provide a defined state on the debug-input pins to the ARC core when the Emulator isn't connected, pull-down resistors should be fitted on the TDI, TMS and TCK pins on the target board (typically 10KΩ).

Note 5: Connect this pin to the Target's System-Reset line (active-low), if available. The Emulator pulls SRESET* low (open-drain) to reset the target; the Emulator also senses a target system reset on this pin. The Target must provide a pull-up to Vcc (minimum 4.7KΩ, maximum 1mA) on this pin. If a System-Reset line is not available, do not connect to this pin.

Table 1: Pin connections on Ashling's TPA-ARC-JTAG-20 Probe Assembly for use with target ARC-core boards

The block-schematic for the **TPA-ARC-JTAG-20** Target Probe Assembly when connected to the Opella-ARC Emulator is shown in Figure 1. "3.3V/2.5V Autoswitch" means that these pins are driven by (or terminated by) 74LVCHR16245 *and* 74AVC16245A buffers in the probe or the emulator. The 74LVCHR16245 buffers are enabled when a target voltage of 3.3V is detected; the 74AVC16245A buffers are enabled when a target voltage of 2.5V is detected (or when no target voltage is detected).

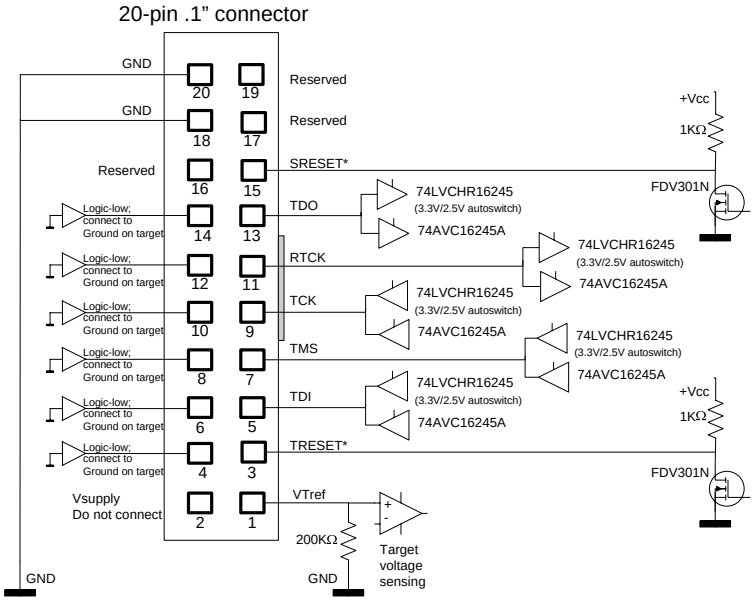

Figure 1. Pin-out of Ashling's TPA-ARC-JTAG-20 Probe Assembly when connected to the Opella-ARC Emulator, for use with target ARC-core boards

The drive capability of the Opella-ARC Emulator when connected to the **TPA-ARC-JTAG-20** Target Probe Assembly is shown in Table 2.

	Load	Low-state	High-state
VTref Output pin (to Emulator from Target): Emulator termination characteristics	200KΩ to ground		
TDI, TMS and TCK Input pins (to Target from Emulator): Emulator drive characteristics		-24mA drive @ 0.55V max; or -100µA drive @ 0.2V max.	+24mA drive @ 2.0V min; or +100µA drive @ Vcc – 0.2V min.
TDO and RTCK Output pins (to Emulator from Target): Emulator termination characteristics	±5 µA termination current	0.7V max.	1.7V min at Vcc 2.3V; 2.0V min at Vcc 2.7V
SRESET* and TRESET* Input pins (to Target from Emulator): Emulator drive characteristics		105Ω @ –2mA max.	1.1KΩ to +3.3V

Table 2: Ashling Opella-ARC Emulator drive and termination characteristics, when connected to TPA-ARC-JTAG-20 Target Probe Assembly

3.2 Connecting to Siano's SMS1000-series ARC-core devices

When debugging the ARC core on Siano's SMS1000-series devices, developers should:

- Ensure that Pin 11 (RTCK) on the Ashling 20-pin debug connector (see Table 1) connects to the RTCK output from the ARC core. Each time that Opella-ARC sends a rising-high TCK signal it will await a rising-high RTCK before continuing.
- Ensure that Pin 15 (SRESET*) on the Ashling 20-pin debug connector (see Table 1) connects to the Reset (active-low) output from the ARC core, so that a Reset can be detected by Opella-ARC;
- Select the Siano target option from the Ashling DRI-SeeCode-ARC driver software's Configuration dialog, so that Opella-ARC will respond to RTCK and SRESET* from the target SMS1000 ARC core.

3.3 Connecting to the target system's Reset line

The System-Reset circuit on the target ARC application must allow the *SRESET pin on the Ashling 20-pin debug connector to both assert and sense a Reset on the target system.

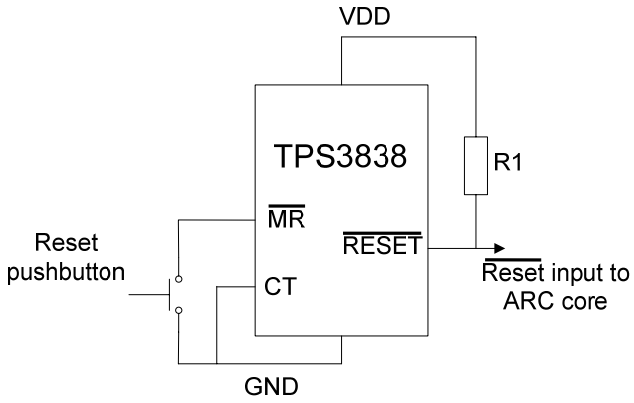

Figure 2. A typical System-Reset circuit

Figure 2 shows a typical Reset circuit, implemented using a TI TPS3838 power-supervision device. The device holds its RESET* output low for a predetermined time after power is sensed on the Vdd pin; in addition, an active-low signal, such as a pushbutton, on the MR* input will assert RESET* low. In this schematic, the *SRESET pin on the Ashling 20-pin debug connector can be connected *either* to the MR* pin *or* to the RESET* pin on the TPS3838 device. Because the TPS3838 has an active-low open-drain output, the Opella-ARC unit can both sense a Reset condition as a Low state on MR* or RESET*, and it can assert a Reset on the target by pulling either MR* or RESET* low.

3.4 Alternative ARCangel Debug and FPGA blasting probe connections

For debugging on the ARCangel prototyping platform (or on user boards that use the same connection scheme as ARCangel, using 3.3V logic levels on the debug interface), Ashling supplies a 15-pin debug probe cable.

Ashling's **TPA-ARC-JTAG-15** Target Probe Assembly contains a D15 Male free plug (see Figure 3) that connects to the D15 Female fixed socket on ARCangel. Pin connections for this connector are shown in tabular form in Table 3.

Pin	*Signal*	*Function (Debugging and FPGA Flashing on ARCangel board)*	*Function (Debugging only)*	*Direction*
1	FPGA_DATA (D0)	Downloaded FPGA data (ARCangel only)	Unused	Input (to Target from Emulator)
2	FPGA_CLK (D1)	FPGA programming clock (ARCangel only)	Unused	Input (to Target from Emulator)
3	Unused (D2)			
4	Unused (D3)			
5	Unused (D4)			
6	SS0	ARCangel configuration bit 0 (ARCangel only)	ARCangel configuration bit 0 (ARCangel only)	Input (to Target from Emulator)
7	SS1 (RESET)	ARCangel configuration bit 1 (RESET) (ARCangel only)	ARCangel configuration bit 1. Pulling this pin low will reset the ARC target. (ARCangel only)	Input (to Target from Emulator)
8	CNT	ARCangel control (ARCangel only)	ARCangel control (ARCangel only)	Input (to Target from Emulator)
9	DONE (OP)	ARCangel FPGA programmed OK (ARCangel only)	Unused	Output (from Target to Emulator)
10	TDI	JTAG test data in	JTAG test data in	Input (to Target from Emulator)
11	TMS	JTAG test data mode in	JTAG test data mode in	Input (to Target from Emulator)
12	TDO	JTAG test data out	JTAG test data out	Output (from Target to Emulator)
13	GND	Ground	Ground	
14	TCK	JTAG clock	JTAG clock	Input (to Target from Emulator)
15	GND	Ground	Ground	

Table 3: Pin connections on Ashling's TPA-ARC-JTAG-15 Probe Assembly for use with ARCangel

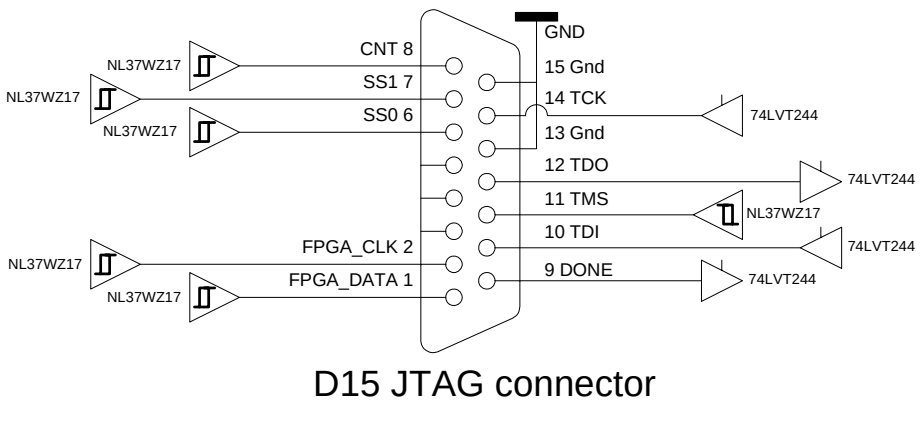

Figure 3. Pin-out of Ashling D15 JTAG Probe, for use with ARCangel

The drive capability of the TPA-ARC-JTAG-15 Emulator Probe is shown Table 4.

	Load	Low-state	High-state
Input pins 1, 2, 6, 7, 8, 11 (to Device from Emulator): Emulator drive characteristics		-24mA drive @ 0.55V max; or -100µA drive @ 0.1V max.	+24mA drive @ 2.3V min; or +100µA drive @ 3.2V min.
Input pins 10, 14 (to Device from Emulator): Emulator drive characteristics		-32mA drive @ 0.5V max; or -100µA drive @ 0.2V max.	+32mA drive @ 2.0V min; or +100µA drive @ 3.1V min.
Output pins 9, 12 (to Emulator from Device): Emulator termination characteristics	±500 µA termination current while switching	0.8V max.	2.0V min.

Table 4: Ashling D15 JTAG Probe drive and termination characteristics

The on-chip driver and receiver pads, and the on-chip and off-chip pull-up or pull-down resistors, must be chosen so as to ensure adequate signal transitions to the Emulator (on Output pins) and to correctly sense logic voltages from the Emulator (on Input pins). The ARCangel prototyping system (section 7) meets these requirements.

4 ARC-core Target Debug Connector

The recommended Debug Connector is available in a variety of styles. As a typical example, for the 20-way Debug Connector, target ARC-core boards can use a 20-way IDC male header, 0.1" pitch, such as AMP part numbers 1437045-2 (vertical) or 9-1437044-5 (right angle).

5 Target voltage interfacing

The Ashling tools for ARC-core debugging support 1.8V, 2.5V and 3.3V target systems, when connected to the target using the **TPA-ARC-JTAG-20** 20-pin .1" Target Probe Assembly. The emulators automatically adjust their logic interface levels to cater for the target's levels. The **TPA-ARC-JTAG-15 D15** Target Probe Assembly supports ARCangel (or ARC core) targets at 3.3V.

6 Installing and Configuring the SeeCode Debugger for use with Opella-ARC

Ashling's Opella-ARC Emulator is supplied with software that installs the USB driver (for the connection to the host PC), together with a diagnostic utility that verifies the connection to the target ARC core, optionally downloads the FPGA build, and tests that the ARC core is responding. For Ashling's latest Opella-ARC software, see www.arcadisystems.com/support/arc

You should run "Setup" from this software before using Opella-ARC. ARC's SeeCode debugger includes Options dialogs that directly support Opella-ARC. Choose **Target-specific Options**, then select **Hardware** as the target and **Ashling Opella JTAG for ARC** as the hardware connection.

It's best to set up your system initially with a low JTAG clock frequency, such as 750KHz. Once you have established communication with the target, you can increase the JTAG clock to the highest

frequency that maintains stable, consistent operation of the emulator and debugger. You should not select a JTAG frequency that is more than half of the ARC core processor's clock frequency. If you need to operate the JTAG clock at a very low frequency on a power-conscious design, please note that operation of the debugger at lower JTAG frequencies will be slow!

7 The ARCangel development platform

Figure 4. ARC's ARCangel-4 Development platform

ARC's ARCangel prototyping system is an FPGA-based development platform for hardware and software co-development and co-verification that allows hardware engineers and software programmers to evaluate, test and verify a SoC design based on the ARC processor core before committing the final design to silicon (Figure 4).

The ARC core architecture and tools-set allows a designer to customize the ARC core's instruction-set to optimize their system's performance. ARCangel supports the prototyping of integrated custom instructions, custom interfaces, RAM, DIMM or Flash memories, multiple processor systems, and additional IP blocks. Ethernet, USB and Bluetooth interfaces are implemented using on-board resources or upgrade boards.

The Ashling Opella-ARC Emulator connects to ARCangel-3 and ARCangel-4 using the Ashling ARC D15 JTAG Probe Cable (part number TPA-ARC-JTAG-15); this probe has a male D15 connector that plugs directly into the D15 JTAG female socket on ARCangel.

The Configuration DIPswitch on the ARCangel-4 system must be set as follows:

DIPswitch 2 OFF (select Passive serial CFG mode; factory-default is ON)
DIPswitch 5 ON (select ARC JTAG communications on D15 connector; factory-default is OFF)

The switches on the back panel of the ARCangel-3 prototyping system must be set up as follows:

Switch 2 Off (select Serial mode)
Switch 5 On (select Alternate DB15 JTAG connection).

8 References

Further details on JTAG and on the ARCangel prototyping system can be found at:

1. IEEE Standard 1149.1 (Test Access Port and Boundary Scan Architecture) can be purchased from http://www.ieee.org/web/standards/home/index.html
2. www.arc.com/software/evalsystems/

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