

# Ashling Opella-XD for ARC

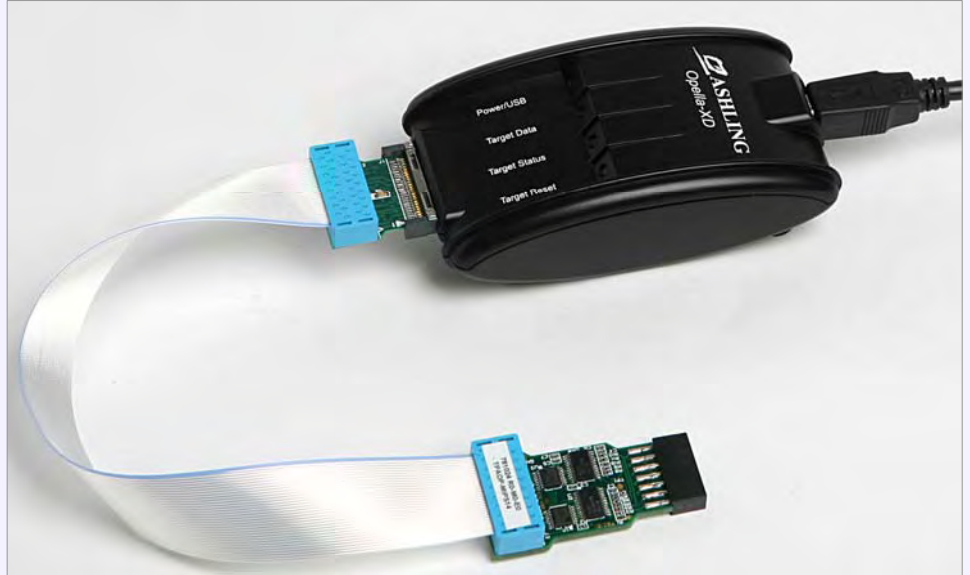
## *Ultra-high-speed JTAG Debug Probe*

Ashling's **Opella-XD JTAG Debug Probe**, supplied and supported by Arcadi Systems, is the fastest-available debug probe for embedded development with ARC International's ARC™ configurable RISC cores.

Developed in cooperation with ARC International plc, the Opella-XD probe integrates with ARC's SeeCode or GNU GDB Debuggers under Windows™ or Linux hosts.

Advanced features of Opella-XD include:

- Fast, easy-to-install USB 2.0 High-Speed Interface (480Mb/s)
- Supports all popular hardware debug protocols
- Works with Windows and Linux hosts
- Hot-plug support allows post-mortem debugging
- Fast, trouble-free Plug-and-Play installation
- Supplied with 20-pin .1" Target Probe Assembly for Debug interface to target device or target FPGA
- Versatile Target-Reset and Test-Port-Reset support
- Built-in diagnostics instantly show status of Target, Debug Probe and USB link
- Unique Auto-conditioning Probe provides maximum possible download speed to target with fastest JTAG clock frequencies
- Optional 15-pin D-Type JTAG adapter for Debug interface to target device or ARCAngel prototyping system
- Wide target voltage range: 0.9V to 3.6V
- Supports FPGA Programming on ARC FPGA targets, including ARCAngel, or on user's target board



Used together with the **ARC SeeCode** or **GNU GDB ARC** Debuggers, Opella-XD-ARC provides a complete Emulation, Code-download, Source Debugging and FPGA programming workbench for development of embedded systems based on any of ARC's Configurable RISC Cores.

Benefits of **Opella-XD** to the embedded hardware developer include:

- Accelerates the entire embedded-hardware debug process: ultra-fast installation, code download and flash programming saves time at every code rebuild
- Instantly auto-configures to target system
- Long-term investment: works with all popular target architectures and compilers
- Helps with the most difficult debugging tasks: hardware bring-up, operating-system boot, post-mortem debugging
- Future-proof: works with latest hardware-debug protocols, all popular host operating-systems
- Compact, easy-to-install target probe cables support all popular debug interfaces

*ARC, ARCAngel and ARCAngel are trademarks or registered trademarks of ARC International plc*

## Opella-XD Debug Probe Specification

- High-speed USB2.0 (480Mb/s) interface to host PC or Linux workstation
- Target JTAG clock rates up to 100MHz
- Auto-conditioning Probe Cable for fast JTAG clock frequencies
- Sustained code download to target at over 3MB/s (using 100MHz JTAG clock)
- 20-way IDC or 15-way D-type target JTAG connectors
- Configurable Target-Reset and Test-Port-Reset, under full user control
- Fine-grained adjustment of JTAG clock frequency from 1KHz to 100MHz
- Supports target operating voltages from 0.9V to 3.6V. Opella-XD detects and automatically configures for the appropriate target voltage.
- Run/stop control of target application including go, halt, step-over, step-into and step-out-of
- Supports RTCK adaptive clocking of debug data from target
- “Hot-plug” support; allows connection to a running target without resetting or halting
- Fully powered by USB interface; no external power-supply is needed
- Operates with ARC’s SeeCode or GNU GDB Debuggers under Windows™ or Linux hosts
- Support for Multi-core debugging
- Support for multiple Opella units connected to a single PC or workstation, for multiple cores with multiple JTAG ports
- Support for FPGA programming on the ARCangel™ prototyping system or target ARC-core FPGA device

## Target Connection

20-pin .1” Target Probe Assembly for Debug interface to target ARC-core device or target FPGA. Optional 15-pin D-Type JTAG target probe adapter for Debug interface to ARCangel prototyping system.

## Device Support

All ARC cores with a JTAG Debug Interface are supported, including ARC 600, ARC 700, Energy Pro EP20 and EP30, ARCtangent-A4 and ARCtangent-A5; the ARCangel Prototyping System is also supported.

## Product configuration

Each Opella-XD-ARC product package includes:

Opella-XD-ARC High-performance JTAG Emulator; 20-pin .1” Target Probe Assembly; USB cable; documentation.

The Ashling DRI-XD-SeeCode-ARC software driver package is ordered separately. The software package includes both Windows- and Linux-hosted drivers, and operates with the ARC SeeCode or GNU GDB ARC debuggers. A 15-pin D-Type target socket adapter is available as an option, for use with the ARCangel prototyping system.

## Order Codes

Product	Order Code
<b>Opella-XD-ARC High-Performance Debug Probe.</b> Includes TPAOP-ARC20 target cable, USB 2.0 cable and documentation. Requires DRI-XD-SeeCode-ARC driver software.	Opella-XD-ARC
<b>DRI-XD-SeeCode-ARC software drivers.</b> To connect Opella-XD to ARC SeeCode Debugger or GNU GDB ARC open-source debugger, on Windows and Linux hosts	DRI-XD-SeeCode-ARC
<b>TPAOP-ARC20 Probe Cable,</b> with 20-pin 0.1”-pitch IDC connector. Supports target voltages 0.9V to 3.6V. Included with Opella-XD-ARC.	TPAOP-ARC20
<b>AD-ARC-D15 Adapter,</b> used with TPAOP-ARC20 probe cable to connect to 15-pin connector on ARCangel prototyping system	AD-ARC-D15

*Ashling Microsystems Ltd. reserves the right to alter product specifications at any time and without notice*



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